UNITRODE

APPLICATION NOTE

UC3854 Controlled Power Factor Correction Circuit Design

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ABSTRACT

This Application Note describes the concepts and design of a boost preregulator for power factor correction. This note covers the important specifications for power factor correction, the boost power circuit design and the UC3854 integrated circuit which controls the converter. A complete design procedure is given which includes the tradeoffs necessary in the process. This design procedure is directly applicable to the UC3854A/B as well as the UC3854. The recommendations in Unitrode Design Note DN-39 cover other areas of the circuit and, while not discussed here, must be considered in any design. This application note supersedes Application Note U- 125 "Power Factor Correction With the UC3854. "

INTRODUCTION

The objective of active power factor correction is to make the input to a power supply look like a simple resistor. An active power factor corrector does this by programming the input current in response to the input voltage. As long as the ratio between the voltage and current is a constant the input will be resistive and the power factor will be 1.0. When the ratio deviates from a constant the input will contain phase displacement, harmonic distortion or both and either one will degrade the power factor.

The most general definition of power factor is the ratio of real power to apparent power.

$$PF = \frac{P}{(Vrms \times Irms)} \text{ or } PF = \frac{Watts}{V.A.}$$

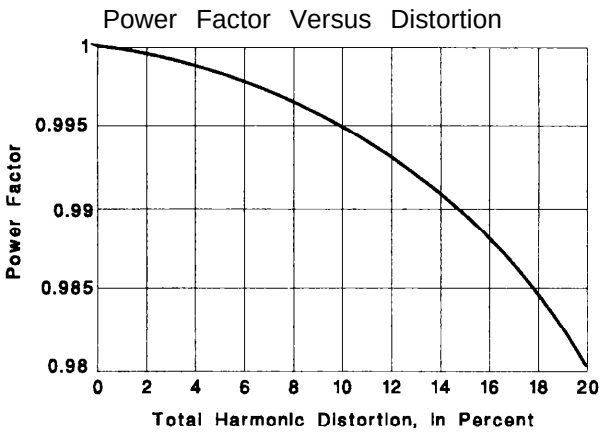
Where P is the real input power and Vrms and Irms are the root mean square (RMS) voltage and current of the load, or power factor corrector input in this case. If the load is a pure resistance the real power and the product of the RMS voltage and current will be the same and the power factor will be 1.0. If the load is not a pure resistance the power factor will be below 1.0.

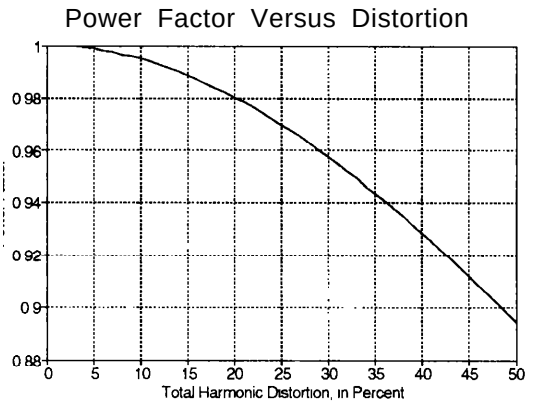
Phase displacement is a measure of the reactance of the input impedance of the active power factor corrector. Any amount of reactance, either inductive or capacitive will cause phase displacement of the input current waveform with respect to the input voltage waveform. The phase displacement of the voltage and current is the classic definition of power factor which is the cosine of the phase angle between the voltage and current sinusoids.

$$PF = \cos\theta$$

The amount of displacement between the voltage and current indicates the degree to which the load is reactive. If the reactance is a small part of the impedance the phase displacement will be small. An active power factor corrector will generate phase displacement of the input current if there is phase shift in the feedforward signals or in the control loops. Any filtering of the AC line current will also produce phase displacement.

Harmonic distortion is a measure of the non-linearity of the input impedance of the active power factor corrector. Any variation of the input impedance as a function of the input voltage will cause distortion of the input current and this distortion is the other contributor to poor power factor. Distortion increases the RMS value of the current without increasing the total power being drawn. A non-linear load will therefore have a poor power factor because the RMS value of the current is high but the total power delivered is small. If the non-linearity is small the harmonic distortion will be low. Distortion in an active power factor corrector comes from





Harmonic Order	Permissible current	Maximum permissible current
n	mA/W	A
Odd harmonics		
3	3.4	2.30
5	1.9	1.14
7	1.0	0.78
9	0.5	0.40
11	0.35	0.33
13	0.3	0.21
15 up	3.85/n	$0.15 \times \frac{15}{n}$
Even harmonics		
2	1.8	1.08
4	0.7	0.42
6	0.5	0.30
>8	$\frac{3}{n}$	$\frac{1.80}{n}$

Table 1

several sources: the feedforward signals, the feedback loops, the output capacitor, the inductor and the input rectifiers.

An active power factor corrector can easily achieve a high input power factor, usually much greater than 0.9. But power factor is not a sensitive measure of the distortion or the displacement of the current waveform. It is often more convenient to deal with these quantities directly rather than with the power factor. For example, 3% harmonic distortion alone has a power factor of 0.999. A current with 30% total harmonic distortion still has a power factor of 0.95. A current with a phase displacement of 25 degrees from the voltage has a power factor of 0.90.

The trend among the world standards organizations responsible for power quality is to specify maximum limits for the amount of current allowed at each of the harmonics of the line frequency. IEC 555-2 specifies each harmonic up through and beyond the 15th and the amount of current permissible at each. Table 1 lists the requirements for IEC 555-2 as of the time of this writing. There are two parts to the specification, a relative distortion and an absolute distortion maximum. Both limits apply to all equipment. This table is included here as an example of a line distortion specification. It is not intended to be used for design purposes. The IEC has not finalized the requirements of IEC 555 at this time and major changes are possible.

Active Power Factor Correction

A boost regulator is an excellent choice for the power stage of an active power factor corrector because the input current is continuous and this produces the lowest level of conducted noise and the best input current waveform. The disadvantage of the boost regulator is the high output voltage required. The output voltage must be greater than the highest expected peak input voltage.

The boost regulator input current must be forced or programmed to be proportional to the input voltage waveform for power factor correction. Feedback is necessary to control the input current and either

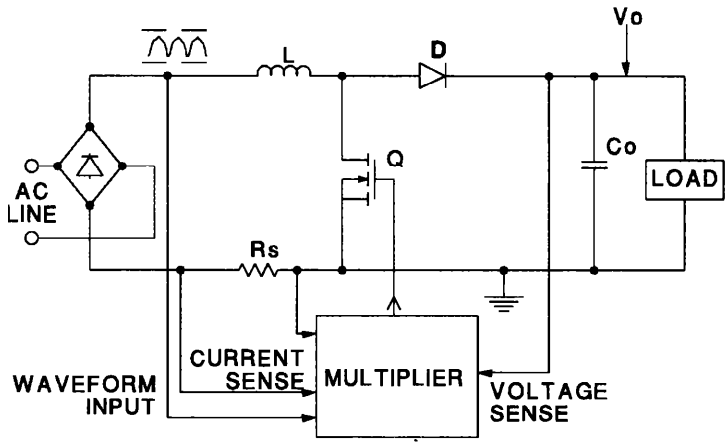


Figure 1

Basic Configuration of High Power Factor Control Circuit

peak current mode control or average current mode control may be used. Both techniques may be implemented with the UC3854. Peak current mode control has a low gain, wide bandwidth current loop which generally makes it unsuitable for a high performance power factor corrector since there is a significant error between the programming signal and the current. This will produce distortion and a poor power factor.

Average current mode control is based on a simple concept. An amplifier is used in the feedback loop around the boost power stage so that input current tracks the programming signal with very little error. This is the advantage of average current mode control and it is what makes active power factor correction possible. Average current mode control is relatively easy to implement and is the method described here.

A block diagram of a boost power factor corrector circuit is shown in Figure 1. The power circuit of a

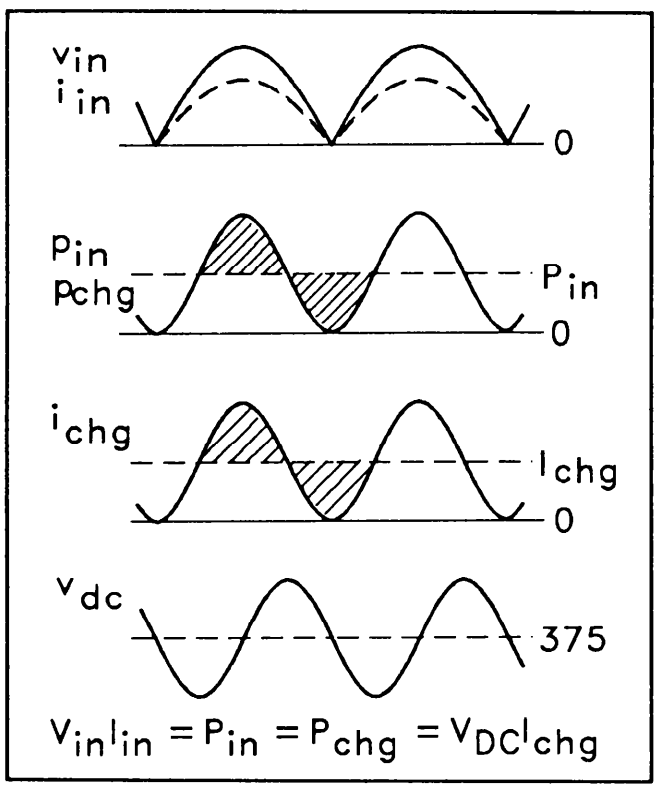


Figure 2. Preregulator Waveforms

boost power factor corrector is the same as that of a dc to dc boost converter. There is a diode bridge ahead of the inductor to rectify the AC input voltage but the large input capacitor which would normally be associated with the AC to DC conversion function has been moved to the output of the boost converter. If a capacitor follows the input diode bridge it is a small one used only for noise control.

The output of the boost regulator is a constant voltage but the input current is programmed by the input voltage to be a half sine wave. The power flow into the output capacitor is not constant but is a sine wave at twice the line frequency since power is the instantaneous product of voltage an current. This is shown in Figure 2. The top waveform shows the voltage and the current into the power factor corrector and the second waveform shows the flow of energy into and out of the output capacitor. The output capacitor stores energy when the input voltage is high and releases the energy when the input voltage is low to maintain the output power flow. The third waveform in Figure 2 shows the charging and discharging current. This current has a different shape from the input current and is almost entirely at the second harmonic of the AC line voltage. This flow of energy into and out of the capacitor results in ripple voltage at the second harmonic also and this is shown in the fourth waveform in Figure 2. Note that the voltage ripple is displaced by 90 degrees relative to the current since this is reactive energy storage. The output capacitor must be rated to handle the second harmonic ripple current as well as the high frequency ripple current from the boost converter switch which modulates it.

Control Circuits

An active power factor corrector must control both the input current and the output voltage. The current loop is programmed by the rectified line voltage so that the input to the converter will appear to be resistive. The output voltage is controlled by changing the average amplitude of the current programming signal. An analog multiplier creates the current programming signal by multiplying the rectified line voltage with the output of the voltage error amplifier so that the current programming signal has the shape of the input voltage and an average amplitude which controls the output voltage. Figure 3 is a block diagram which shows the basic control circuit arrangement necessary for an active power factor corrector. The output of the multiplier is the current programming signal and is called Imo for multiplier output current. The multiplier input from the rectified line voltage is shown as a current in Figure 3 rather than as a voltage signal because this is the way it is done in the UC3854.

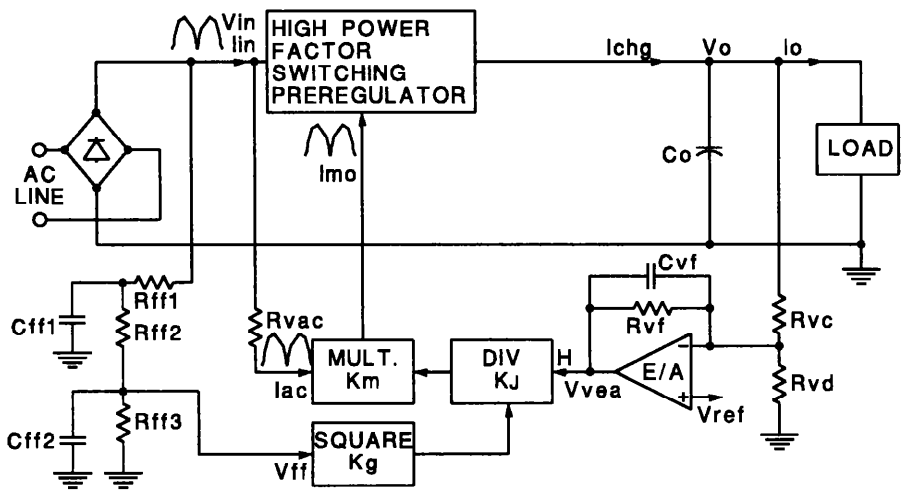


Figure 3. High Power Factor

Figure 3 shows a squarer and a divider as well as a multiplier in the voltage loop. The output of the voltage error amplifier is divided by the square of the average input voltage before it is multiplied by the rectified input voltage signal. This extra circuitry keeps the gain of the voltage loop constant, without it the gain of the voltage loop would change as the square of the average input voltage. The average value of the input voltage is called the feedforward voltage or Vff since it provides an open loop correction which is fed forward into the voltage loop. It is squared and then divided into the voltage error amplifier output voltage (Vvea).

The current programming signal must match the rectified line voltage as closely as possible to maximize the power factor. If the voltage loop bandwidth were large it would modulate the input current to keep the output voltage constant and this would distort the input current horribly. Therefore the voltage loop bandwidth must be less than the input line frequency. But the output voltage transient response must be fast so the voltage loop bandwidth must be made as large as possible. The squarer and divider circuits keep the loop gain constant so the bandwidth can be as close as possible to the line frequency to minimize the transient response of the output voltage. This is especially important for wide input voltage ranges.

The circuits which keep the loop gain constant make the output of the voltage error amplifier a power control. The output of the voltage error amplifier actually controls the power delivered to the load. This can be seen easily from an example. If the output of the voltage error amplifier is constant and the input voltage is doubled the programming signal will double but it will be divided by the square of the feedforward voltage, or four times the input, which will result in the input current being reduced to half its original value. Twice the input voltage times half the input current results in the same input power as before. The output of the voltage error amplifier, then, controls the input power level of the power factor corrector. This can be used to limit the maximum power which the circuit can draw from the power line. If the output of the voltage error amplifier is clamped at some value that corresponds to some maximum power level, then the active power factor corrector will not draw more than that amount of power from the line as long as the input voltage is within its range.

Input Distortion Sources

The control circuits introduce both distortion and displacement into the input current waveform. These errors come from the input diode bridge, the multiplier circuits and ripple voltage, both on the output and on the feedforward voltage.

There are two modulation processes in an active power factor corrector. The first is the input diode bridge and the second is the multiplier, divider, squarer circuit. Each modulation process generates cross products, harmonics or sidebands between the two inputs. The description of these mathematically can be quite complex. Interestingly enough, however, the two modulators interact and one becomes a demodulator for the other so that the result is quite simple. As shown later, virtually all of the ripple voltages in an active power factor corrector are at the second harmonic of the line frequency. When these voltages go through the multiplier and get programmed into the input current and then go through the input diode bridge the second harmonic voltage amplitude results in two frequency components. One is at the third harmonic of the line frequency and the other is at the fundamental. Both of these components have an amplitude which is half of the amplitude of the original second harmonic voltage. They also have the same phase as the original second harmonic. If the ripple voltage is 10% of the line voltage amplitude and is phase shifted 90 degrees the input current will have a third harmonic which is 5% of the fundamental and is shifted 90 degrees and a fundamental component which is 5% of the line current and is displaced by 90 degrees.

The feedforward voltage comes from the rectified AC line which has a second harmonic component that is 66% of the amplitude of the average value. The filter capacitors of the feedforward voltage divider greatly attenuate the second harmonic and effectively remove all of the higher harmonics but some of the second harmonic is still present at the feedforward input. This ripple voltage is squared by the control circuits as shown in Figure 3. This doubles the amplitude of the ripple since it is riding on top of a large DC value. The divider process is transparent to the ripple voltage so it passes on to the multiplier and eventually becomes third harmonic distortion of the input current and a phase displacement. The doubling action of the squarer means that the amplitude of the input current distortion in percent is the same as the amplitude of the ripple voltage, in percent, at the feedforward input.

Needless to say, the feedforward ripple voltage must be kept small to achieve a low distortion input current. The ripple voltage could be made small with a single pole filter with a very low cutoff frequency. However, fast response to changes of the input voltage is also desirable so the response time of the filter must be fast. These two requirements are, of course, in conflict and a compromise must be found. A two pole filter on the feedforward input has a faster transient response than a single pole filter for the same amount of ripple attenuation. Another advantage of the two pole filter has is that the phase shift is twice that of the single pole filter. This results in 180 degrees of phase shift of the second harmonic and brings both the resulting third harmonic and the displacement component of the input current back in phase with the voltage. A second harmonic ripple voltage of 3% at the feedforward input results in a 0.97 power factor just from the displacement component if a single pole filter is used for the feedforward voltage. With a two pole filter there is no displacement component to the power factor because it is in

phase with the input current. The third harmonic component of the input current resulting from the second harmonic at the feedforward input will have the same amplitude as the second harmonic ripple voltage. If 3% second harmonic is present on the feedforward voltage the line current waveform will contain 3% third harmonic distortion.

The output voltage has ripple at the second harmonic due to the ripple current flowing through the output capacitor. This ripple voltage is fed back through the voltage error amplifier to the multiplier and, like the feedforward voltage, programs the input current and results in second harmonic distortion of the input current. Since this ripple voltage does not go through the squarer the amplitude of the distortion and displacement are each half of the amplitude of the ripple voltage. The ripple voltage at the output of the voltage error amplifier must be in phase with the line voltage for the displacement component to be in phase. The voltage error amplifier must shift the second harmonic by 90 degrees so that it will be in phase with the line voltage.

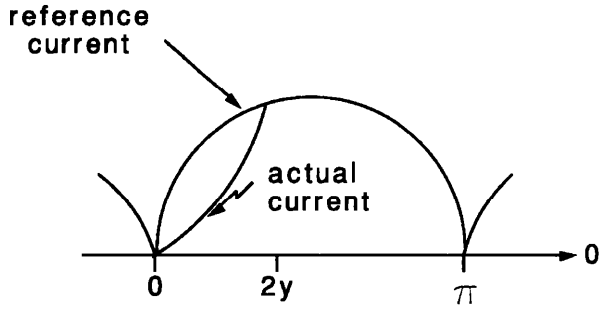


Figure 4. Cusp Distortion

The voltage loop of a boost converter with average current mode control has a control to output transfer function which has a single pole roll off characteristic so it could be compensated with a flat gain error amplifier. This produces a very stable loop with 90 degrees of phase margin. However, it provides less than optimum performance. The ripple voltage on the output capacitor is out of phase with the input current by 90 degrees. If the error amplifier has flat gain at the second harmonic frequency the distortion and displacement generated in the input current will be 90 degrees out of phase with the rectified AC line. The power factor can be improved by introducing phase shift into the voltage error amplifier response. This shifts the displacement component of the power factor back into alignment with the input voltage and increases the power factor. The amount of phase shift which can be added is determined by the need to keep the voltage loop stable. If the phase margin is reduced to 45 degrees the phase at the second harmonic will be very close to 90 degrees and this brings the displacement component back in phase with the input voltage.

The bandwidth of the voltage control loop is determined by the amount of input distortion to be contributed by the output ripple voltage. If the output capacitor is small and the distortion must be low then the bandwidth of the loop will be low so that the ripple voltage will be sufficiently attenuated by the error amplifier. Transient response is a function of the loop bandwidth and the lower the bandwidth the slower the transient response and the greater the overshoot. The output capacitor may need to be large to have both fast output transient response and low input current distortion.

The technique used to design the loop compensation is to find the amount of attenuation of the output ripple voltage required in the error amplifier and then work back into the unity gain frequency. The loop will have the maximum bandwidth when the phase margin is the smallest. A 45 degree phase margin is a good compromise which will give good loop stability and fast transient response and which is easy to design. The voltage error amplifier response which results will have flat gain up to the loop unity gain frequency and will have a single pole roll off above that frequency. This gives the maximum amount of attenuation at the second harmonic of the line frequency from a simple circuit, gives the greatest bandwidth and provides a 45 degree phase margin.

Cusp Distortion

Cusp distortion occurs just after the AC line input has crossed zero volts. At this point the amount of current which is required by the programming signal exceeds the available current slew rate. When the input voltage is near zero there is very little voltage across the inductor when the switch is closed so the current cannot ramp up very quickly so the available slew rate is too low and the input current will lag behind the desired value for a short period of time. Once the input current matches the programmed value the control loop is back in operation and the input current will follow the programming signal. The length of time that the current does not track the programmed value is a function of the inductor value. The smaller the inductor value the better the tracking and the lower the distortion but the smaller inductor value will have higher ripple current. The amount of distortion generated by this condition is generally small and is mostly higher order harmonics. This problem is minimized by a sufficiently high switching frequency.

UC3854 Block Diagram

A block diagram of the UC3854 is shown in Figure 5 and is the same as the one in the device data sheet. This integrated circuit contains the circuits necessary to control a power factor corrector. The UC3854 is designed to implement average current mode control but is flexible enough to be used for a wide variety of power topologies and control methods.

The top left corner of Figure 5 contains the under voltage lock out comparator and the enable comparator. The output of both of these comparators must be true to allow the device to operate. The inverting input to the voltage error amplifier is connected to pin 11 and is called Vsens. The diodes shown around the voltage error amplifier are intended to represent the functioning of the internal circuits rather than to show the actual devices. The diodes shown in the block diagram are ideal diodes and indicate that the non-inverting input to the error amplifier is connected to the 7.5Vdc reference voltage under normal operation but is also used for the slow start function. This configuration lets the voltage control loop begin operation before the output voltage has reached its operating point and eliminates the turn-on overshoot which plagues many power supplies. The diode shown between pin 11 and the inverting input of the error amplifier is also an ideal diode and is shown to eliminate confusion about whether there might be an extra diode drop added to the reference or not. In the actual device we do it with differential amplifiers. An internal current source is also provided for charging the slow start timing capacitor.

The output of the voltage error amplifier, Vvea, is available on pin 7 of the UC3854 and it is also an input to the multiplier. The other input to the multiplier is pin 6, Iac, and this is the input for the programming wave shape from the input rectifiers. This pin is held at 6.0 volts and is a current input. The feedforward input, Vff, is pin 8 and its value is squared before being fed into the divider input of the multiplier. The Iset current from pin 12 is also used in the multiplier to limit the maximum output current. The output current of the multiplier is Imo and it flows out of pin 5 which is also connected to the non-inverting input of the current error amplifier.

The inverting input of the current amplifier is connected to pin 4, the Isens pin. The output of the current error amplifier connects to the pulse width modulation (PWM) comparator where it is compared to the oscillator ramp on pin 14. The oscillator and the comparator drive the set-reset flip-flop which, in turn, drives the high current output on pin 16. The output voltage is clamped internally to the UC3854 at 15 volts so that power MOSFETs will not have their gates over driven. An emergency peak current limit is provided on pin 2 and it will shut the output pulse off when it is pulled slightly below ground. The reference voltage output is connected to pin 9 and the input voltage is connected to pin 15.

DESIGN PROCESS

Power Stage Design

This analysis of the power stage design makes use of a 250W boost converter as an example. The control circuit for a boost power factor corrector does not change much with the power level of the converter. A 5000 watt power factor corrector will have almost the same control circuits as a 50 watt

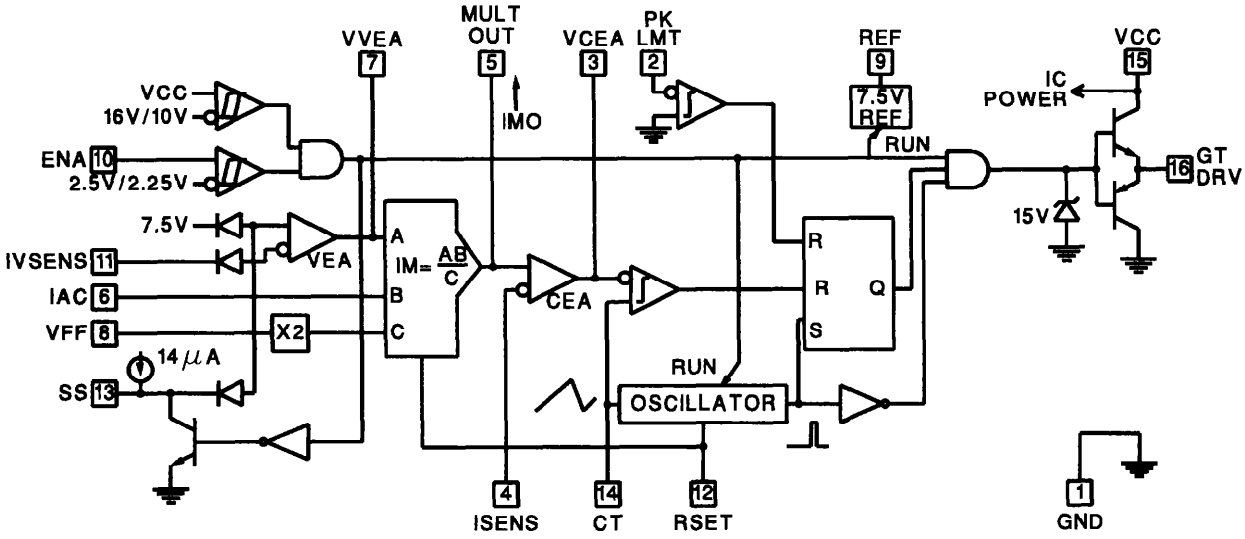


Figure 5. UC3854 Block Diagram

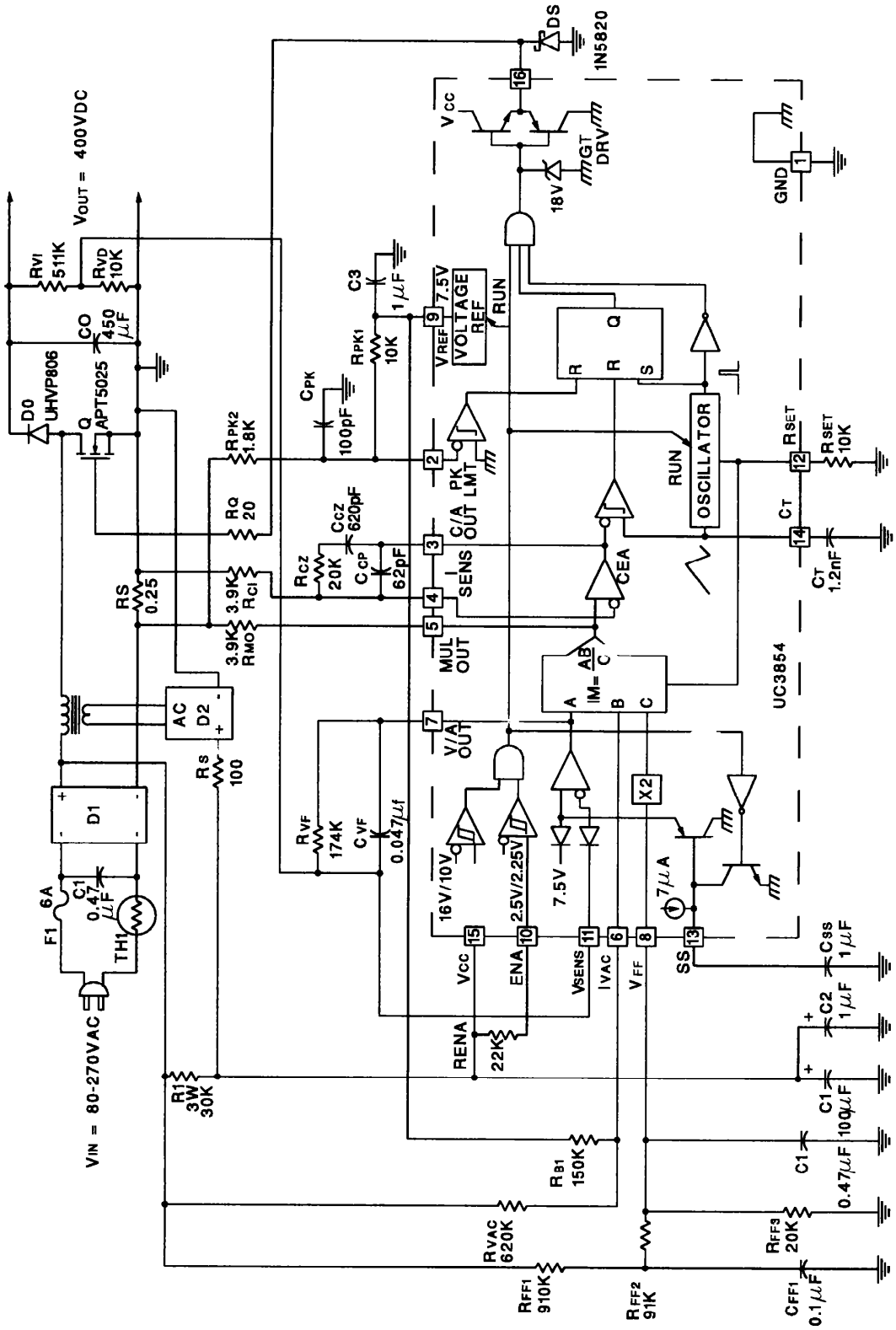


Figure 6.
Complete Schematic of 250W Power Factor Preregulator

corrector. The power stage will be different but the design process will remain the same for all power factor corrector circuits. Since the design process is the same and the power stage is scalable a 250 watt corrector serves well as an example and it can be readily scaled to higher or lower output levels. Figure 6 is the schematic diagram of the circuit. Please refer to this schematic in the discussion of the design process which follows.

Specifications

The design process starts with the specifications for the converter performance. The minimum and maximum line voltage, the maximum output power, and the input line frequency range must be specified. For the example circuit the specifications are:

Maximum power output: 250W

Input voltage range: 80-27OVac

Line frequency range: 47-65Hz

This defines a power supply which will operate almost anywhere in the world. The output voltage of a boost regulator must be greater than the peak of the maximum input voltage and a value 5% to 10% higher than the maximum input voltage is recommended so the output voltage is chosen to be 400Vdc.

Switching Frequency

The choice of switching frequency is generally somewhat arbitrary. The switching frequency must be high enough to make the power circuits small and minimize the distortion and must be low enough to keep the efficiency high. In most applications a switching frequency in the range of 20KHz to 300KHz proves to be an acceptable compromise. The example converter uses a switching frequency of I00KHz as a compromise between size and efficiency. The value of the inductor will be reasonably small and cusp distortion will be minimized, the inductor will be physically small and the loss due to the output diode will not be excessive. Converters operating at higher power levels may find that a lower switching frequency is desirable to minimize the power losses. Turn-on snubbers for the switch will reduce the switching losses and can be very effective in allowing a converter to operate at high switching frequency with very high efficiency.

Inductor Selection

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current. Inductor value selection begins with the peak

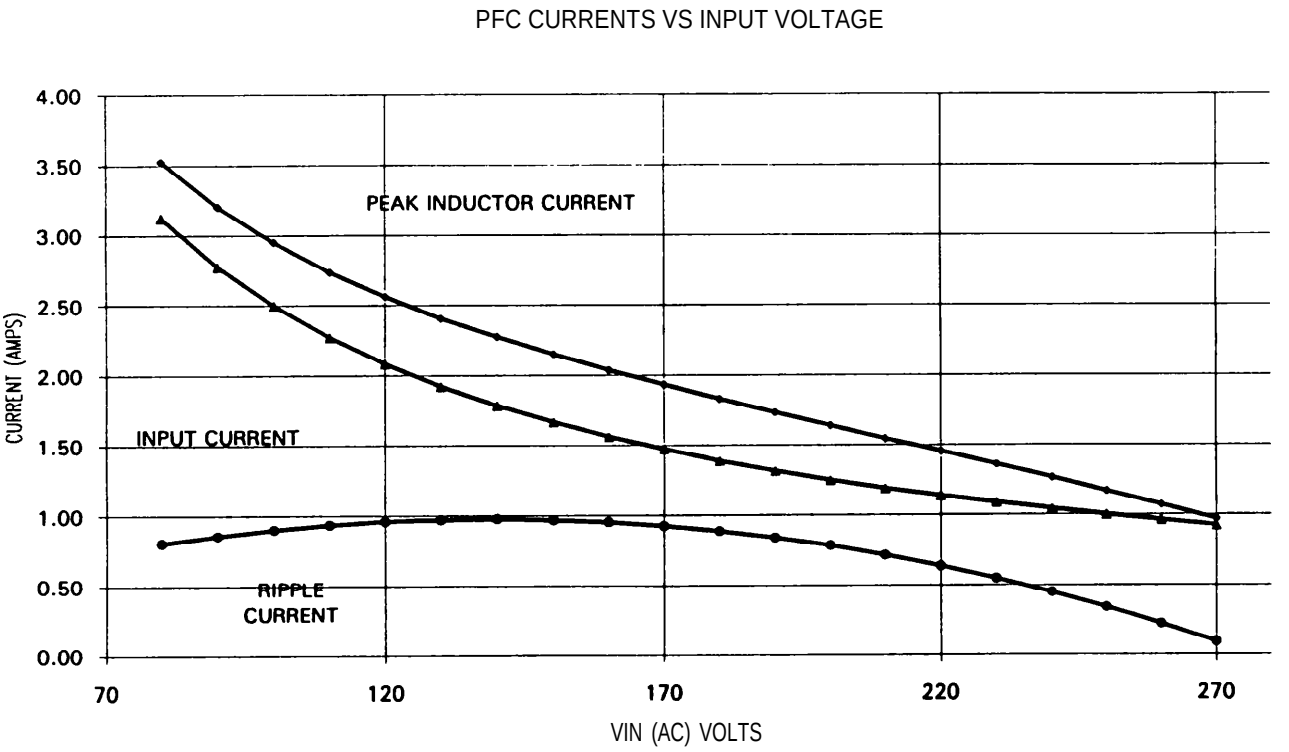


Figure 7

current of the input sinusoid. The maximum peak current occurs at the peak of the minimum line voltage and is given by:

$$I_{line(pk)} = \frac{\sqrt{2} \times P}{Vin(min)}$$

For the example converter the maximum peak line current is 4.42 amps at a Vin of 80Vac.

The maximum ripple current in a boost converter occurs when the duty factor is 50% which is also when the boost ratio M=Vo/Vin=2. The peak value of inductor current generally does not occur at this point since the peak value is determined by the peak value of the programmed sinusoid. The peak value of inductor ripple current is important for calculating the required attenuation of the input filter. Figure 7 is a graph of the peak to peak ripple current in the inductor versus input voltage for the example converter.

The peak-to-peak ripple current in the inductor is normally chosen to be about 20% of the maximum peak line current. This is a somewhat arbitrary decision since this is usually not the maximum value of the high frequency ripple current. A larger value of ripple current will put the converter into the discontinuous conduction mode for a larger portion of the rectified line current cycle and means that the input filter must be larger to attenuate more high frequency ripple current. The UC3854, with average current mode control, allows the boost stage to move between continuous and discontinuous modes of operation without a performance change.

The value of the inductor is selected from the peak current at the top of the half sine wave at low input voltage, the duty factor D at that input voltage and the switching frequency. The two equations necessary are given below:

$$D = \frac{Vo - Vin}{Vo}$$

$$L = \frac{Vin \times D}{fs \times \Delta I}$$

Where ΔI is the peak-to-peak ripple current. In the example 250W converter D=0.71, ΔI=900ma, and L=0.89mH. For convenience the value of L is rounded up to 1.0mH.

The high frequency ripple current is added to the line current peak so the peak inductor current is the sum of peak line current and half of the peak-to-peak high frequency ripple current. The inductor must be designed to handle this current level. For our example the peak inductor current is 5.0 amps. The peak current limit will be set about 10% higher at 5.5 amps.

Output Capacitor

The factors involved in the selection of the output capacitor are the switching frequency ripple current, the second harmonic ripple current, the DC output voltage, the output ripple voltage and the hold-up time. The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the line current. The large electrolytic capacitors which are normally chosen for the output capacitor have an equivalent series resistance which changes with frequency and is generally high at low frequencies. The amount of current which the capacitor can handle is generally determined by the temperature rise. It is usually not necessary to calculate an exact value for the temperature rise. It is usually adequate to calculate the temperature rise due to the high frequency ripple current and the low frequency ripple current and add them together. The capacitor data sheet will provide the necessary ESR and temperature rise information.

The hold-up time of the output often dominates any other consideration in output capacitor selection. Hold-up is the length of time that the output voltage remains within a specified range after input power has been turned off. Hold-up times of 15 to 50 milliseconds are typical. In off-line power supplies with a 400Vdc output the hold-up requirement generally works out to between 1 and 2μF per watt of output. In our 250W example the output capacitor is 450μF. If hold-up is not required the capacitor will be much smaller, perhaps 0.2μF per watt, and then ripple current and ripple voltage are the major concern.

Hold-up time is a function of the amount of energy stored in the output capacitor, the load power, output voltage and the minimum voltage the load will operate at. This can be expressed in an equation to define the capacitance value in terms of the hold-up time.

$$Co = \frac{2 \times Pout \times \Delta t}{Vo^2 - Vo(min)^2}$$

Where Co is the output capacitor, Pout is the load power, Δt is the hold-up time, Vo is the output voltage and Vo(min) is the minimum voltage the load will operate at. For the example converter Pout is 250W, Δt is 64msec, Vo is 400V and Vo(min) is 300V so Co is 450μF.

Switch and Diode

The switch and diode must have ratings which are sufficient to insure reliable operation. The choice of these components is beyond the scope of this Application Note. The switch must have a current rating at least equal to the maximum peak current in

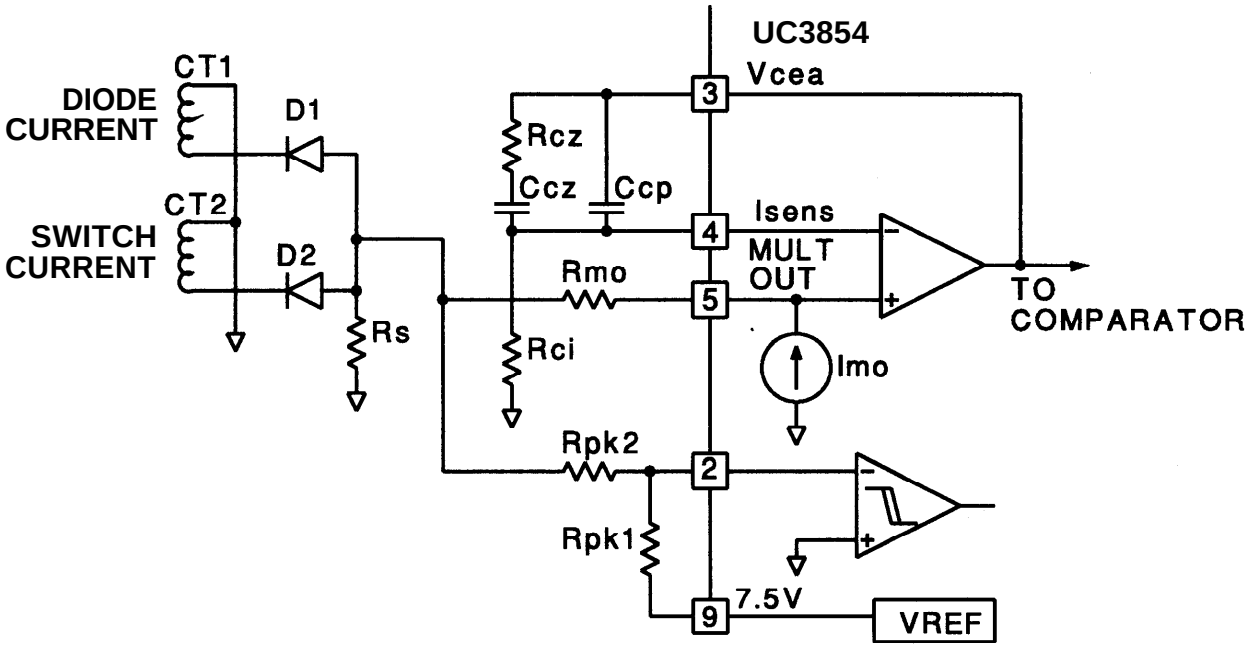


Figure 8.
Current Transformers Used
with Negative Output

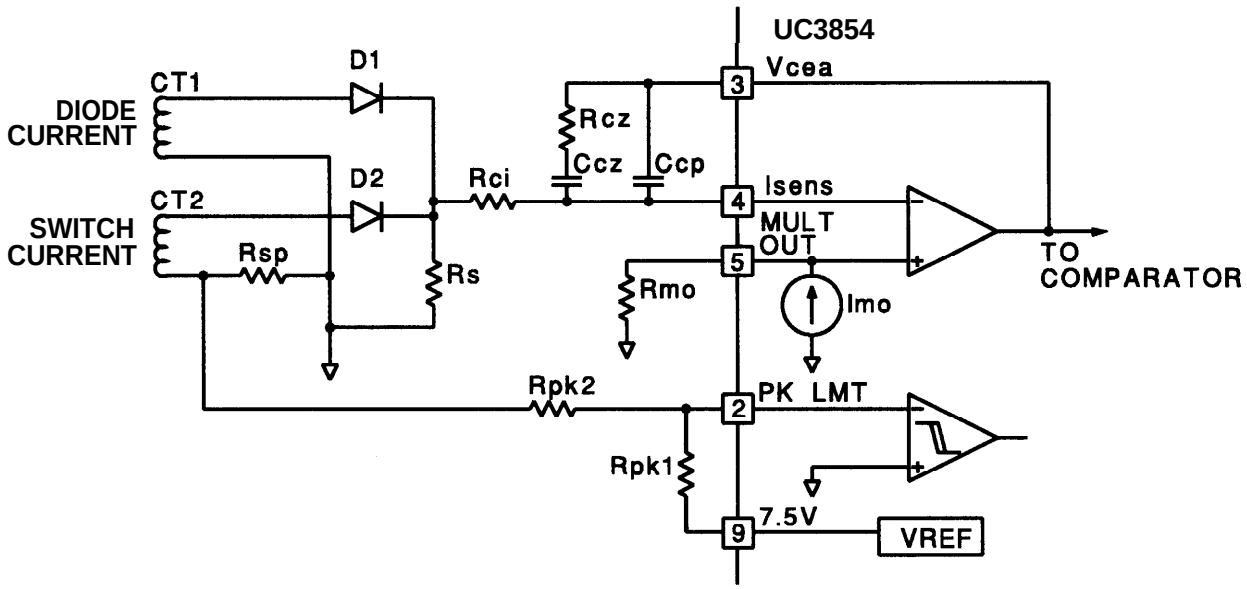


Figure 9.
Current Transformers Used
with Positive Output

the inductor and a voltage rating at least equal to the output voltage. The same is true for the output diode. The output diode must also be very fast to reduce the switch turn-on power dissipation and to keep its own losses low. The switch and diode must have some level of derating and this will vary depending on the application.

For the example circuit the diode is a high speed, high voltage type with 35ns reverse recovery, 600Vdc breakdown, and 8A forward current ratings. The power MOSFET in the example circuit has a 500Vdc breakdown and 23Adc current rating. A major portion of the losses in the switch are due to the turn-off current in the diode. The peak power dissipation in the switch is high since it must carry full load current plus the diode reverse recovery current at full output voltage from the time it turns on until the diode turns off. The diode in the example circuit was chosen for its fast turn off and the switch was oversized to handle the high peak power dissipation. A turn on snubber for the switch would have allowed a smaller switch and a slightly slower diode.

Current Sensing

There are two general methods for current sensing, a sense resistor in the ground return of the converter or two current transformers. The sense resistor is the least expensive method and is most appropriate at low power or current levels. The power dissipation in the resistor may become quite large at higher current levels and in that case the current transformers are more appropriate. Two current transformers are required, one for the switch current and one for the diode current, to produce an analog of the inductor current as is required for average current mode control. The current transformers must operate over a very wide duty factor range and this can be difficult to achieve without saturating them. Current transformer operation is outside the scope of this paper but Unitrode has Design Note DN-41 which discusses the problem in some detail.

The current transformers may be configured for either a positive output voltage or a negative output voltage. In the negative output configuration, shown in Figure 8, the peak current limit on pin 2 of the UC3854 is easy to implement. In the positive output configuration, shown in Figure 9, this feature may be lost. It can be added back by putting another resistor in series with the ground leg of the current transformer which senses the switch current.

The configuration of the multiplier output and the current error amplifier are different depending on whether a resistor is used for current sensing or whether current transformers with positive output voltages are used for current sensing. Both work equally well and the configurations of the current error amplifier are shown in Figures 8 and 9 respectively. The positive output current transformer configuration requires the inverting input to the integrator be connected to the sense resistor and the resistor at the output of the multiplier be connected to ground. (see Figure 9) The voltage at the output of the multiplier is not zero but is the programming voltage for the current loop and it will have the half sine wave shape which is necessary for the current loop.

The resistor current sense configuration is used in the example converter (Figure 6) so the inverting input to the current error amplifier (pin 4) is connected to ground through Rci. The current error amplifier is configured as an integrator at low frequencies for average current mode control so the average voltage at the non-inverting input of the current error amplifier (pin 5, which it shares with the multiplier output) must be zero. The non-inverting input to the current error amplifier acts like a summing junction for the current control loop and adds the multiplier output current to the current from the sense resistor (which flows through the programming resistor Rmo). The difference controls the boost regulator. The voltage at the inverting input of the current error amplifier (pin 4) will be small at low frequencies because the gain at low frequencies is large. The gain at high frequencies is small so relatively large voltages at the switching frequency may be present. But, the average voltage on pin 4 must be zero because it is connected through Rci to ground.

The voltage across Rs, the current sense resistor in the example converter, goes negative with respect to ground so it is important to be sure that the pins of the UC3854 do not go below ground. The voltage across the sense resistor should be kept small and pins 2 and 5 should be clamped to prevent their going negative. A peak value of 1 volt or so across the sense resistor provides a signal large enough to have good noise margin but which is small enough to have low power dissipation. There is a great deal of flexibility in choosing the value of the sense resistor. A 0.25 ohm resistor was chosen for Rs in the example converter and at the worst case peak current of 5.6 amps gives a maximum voltage of 1.40V peak.

Peak Current Limit

The peak current limit on the UC3854 turns the switch off when the instantaneous current through it exceeds the maximum value and is activated when pin 2 is pulled below ground. The current limit value is set by a simple voltage divider from the reference voltage to the current sense resistor.

The equation for the voltage divider is given below:

$$Rpk2 = \frac{Vrs \times Rpk1}{Vref}$$

Where Rpk1 and Rpk2 are the resistors of the voltage divider, Vref is 7.5 volts on the UC3854, and Vrs is the voltage across the sense resistor Rs at the current limit point. The current through Rpk2 should be around 1 mA. The peak current limit in the example circuit is set at 5.4 amps with an Rpk1 of 10K and Rpk2 of 1.8K. A small capacitor, Cpk, has been added to give extra noise immunity when operating at low line and this also increases the current limit slightly.

Multiplier Set-up

The multiplier/divider is the heart of the power factor corrector. The output of the multiplier programs the current loop to control the input current to give a high power factor. The output of the multiplier is therefore a signal which represents the input line current.

Unlike most design tasks where the design begins at the output and proceeds to the input the design of the multiplier circuits must begin with the inputs. There are three inputs to the multiplier circuits: the programming current Iac (pin 6) the feedforward voltage Vff from the input (pin 8) and the voltage error amplifier output voltage Vvea (pin 7). The multiplier output current is Imo (pin 5) and it is related to the three inputs by the following equation:

$$Imo = \frac{Km \times Iac \times (Vvea - 1)}{Vff^2}$$

Where Km is a constant in the multiplier and is equal to 1.0, Iac is the programming current from the rectified input voltage, Vvea is the output of the voltage error amplifier and Vff is the feedforward voltage.

Feedforward Voltage

Vff is the input to the squaring circuit and the UC3854 squaring circuit generally operates with a Vff range of 1.4 to 4.5 volts. The UC3854 has an internal clamp which limits the effective value of Vff to 4.5 volts even if the input goes above that value. The voltage divider for the Vff input has three resistors (Rff1, Rff2 and Rff3 - see Figure 6) and two capacitors (Cff1 and Cff2) and so it filters as well as providing two outputs. The resistors and capacitors of the divider form a second order low pass filter so the DC output is proportional to the average value of the input half sine wave. The average value is 90% of the RMS value of a half sine wave. If the RMS value of the AC input voltage is 270Vac the average value of a half sine will be 243Vdc and the peak will be 382V.

The Vff voltage divider has two DC conditions to meet. At high- input line voltage Vff should not be greater than 4.5 volts. At this voltage the Vff input clamps so the feedforward function is lost. The voltage divider should be set up so that Vff is equal to 1.414 volts when Vin is at its low line value and the upper node of the voltage divider, Vffc, should be about 7.5 volts. This allows Vff to be clamped as described in Unitrode Design Note DN-39B. There is an internal current limit which holds the multiplier output constant if the Vff input goes below 1.414 volts. The Vff input should always be set up so that Vff is equal to 1.414 volts at the minimum input voltage. This may cause Vff to clip on the high end of the input voltage range if there is an extremely wide AC line voltage input range. However, it is preferable to have Vff clip at the high end rather than to have the multiplier output clip on the low end of the range. If Vff clips the voltage loop gain will change but the effect on the overall system will be small whereas the multiplier clipping will cause large amounts of distortion in the input current waveform.

The example circuit uses the UC3854 so the maximum value of Vff is 4.5 volts. If Rff1, the top resistor of the divider, is 910K and Rff2, the middle resistor, is 91 K and Rff3, the bottom resistor, is 20K the maximum value of Vff will be 4.76 volts when the input voltage is 270Vac RMS and the DC average value will be 243 volts. When the input voltage is 80Vac RMS the average value is 72 volts and Vff is 1.41Vdc. Also at Vin=80Vac the voltage at the upper node on the voltage divider, Vffc, will be 7.83 volts. Note that the high end of the range goes above 4.5 volts so that the low end of the range will not go below 1.41 volts.

The output of the voltage error amplifier is the next piece of the multiplier setup. The output of the voltage error amplifier, Vvea, is clamped inside the UC3854 at 5.6 volts. The output of the voltage error amplifier corresponds to the input power of the converter. The feedforward voltage causes the power input to remain constant at given Vvea voltage regardless of line voltage changes. If 5.0V is established as the maximum normal operating level then 5.6V gives an overload power limit which is 12% higher.

The clamp on the output of the voltage error amplifier is what sets the minimum value of Vff at 1.414 volts. This can be seen by plugging these values into the equation for the multiplier output current given above. When Vff is large the inherent errors of the multiplier are magnified because Vvea/Vff becomes small. If the application has a wide input voltage range and if a very low harmonic distortion

is required then Vff may be changed to the range of 0.7 to 3.5 volts. To do this an external clamp MUST be added to the voltage error amplifier to hold its output below 2.00 volts. In general, however, this is not a recommended practice.

Multiplier Input Current

The operating current for the multiplier comes from the input voltage through Rvac. The multiplier has the best linearity at relatively high currents, but the recommended maximum current is 0.6mA. At high line the peak voltage for the example circuit is 382Vdc and the voltage on pin 6 of the UC3854 is 6.0Vdc. A 620K value for Rvac will give an Iac of 0.6mA maximum. For proper operation near the cusp of the input waveform when Vin=0 a bias current is needed because pin 6 is at 6.0Vdc. A resistor, Rb1, is connected from Vref to pin 6 to provide the small amount of bias current needed. Rb1 is equal to Rvac/4. In the example circuit a value of 150K for Rb1 will provide the correct bias.

The maximum output of the multiplier occurs at the peak of the input sine wave at low line. The maximum output current from the multiplier can be calculated from the equation for Imo, given above, for this condition. The peak value of Iac will be 182 microamps when Vin is at low line. Vvea will be 5.0 volts and Vff will be 2.0. Imo will then be 365 microamps maximum. Imo may not be greater than twice Iac so this represents the maximum current available at this input voltage and the peak input current to the power factor corrector will be limited accordingly.

The Iset current places another limitation on the multiplier output current. Imo may not be larger than 3.75 / Rset. For the example circuit this gives Rset = 10.27K maximum so a value of 10K is chosen.

The current out of the multiplier, Imo, must be summed with a current proportional to the inductor current to close the voltage feedback loop. Rmo, a resistor from the output of the multiplier to the current sense resistor, performs the function and the multiplier output pin becomes the summing junction. The average voltage on pin 5 will be zero under normal operation but there will be switching frequency ripple voltage which is amplitude modulated at twice the line frequency. The peak current in the boost inductor is to be limited to 5.6 amps in the example circuit and the current sense resistor is 0.25 ohms so the peak voltage across the sense resistor is 1.4 volts. The maximum multiplier output current is 365 microamps so the summing resistor, Rmo, must be 3.84K and a 3.9K resistor is chosen.

Oscillator Frequency

The oscillator charging current is Iset and is determined by the value of Rset and the oscillator frequency is set by the timing capacitor and the charging current. The timing capacitor is determined from:

$$Ct = \frac{1.25}{Rset \times fs}$$

Where Ct is the value of the timing capacitor and fs is the switching frequency in Hertz. For the example converter fs is 100KHz and Rset is 10K so Ct is 0.00125µF.

Current Error Amplifier Compensation

The current loop must be compensated for stable operation. The boost converter control to input current transfer function has a single pole response at high frequencies which is due to the impedance of the boost inductor and the sense resistor (Rs) forming a low pass filter. The equation for the control to input current transfer function is:

$$\frac{Vrs}{Vcea} = \frac{Vout \times Rs}{Vs \times sL}$$

Where Vrs is the voltage across the input current sense resistor and Vcea is the output of the current error amplifier. Vout is the DC output voltage, Vs is the peak-to-peak amplitude of the oscillator ramp, sL is the impedance of the boost inductor (also jwL), and Rs is the sense resistor (with a current transformer it will be Rs/N). This equation is only valid for the region of interest between the resonant frequency of the filter (LCo) and the switching frequency. Below resonance the output capacitor dominates and the equation is different.

The compensation of the current error amplifier provides flat gain near the switching frequency and uses the natural roll off of the boost power stage to give the correct compensation for the total loop. A zero at low frequency in the amplifier response gives the high gain which makes average current mode control work. The gain of the error amplifier near the switching frequency is determined by matching the down slope of the inductor current when the switch is off with the slope of the ramp generated by the oscillator. These two signals are the inputs of the PWM comparator in the UC3854.

The downslope of the inductor current has the units of amps per second and has a maximum value when the input voltage is zero. In other words, when the voltage differential between the input and output of the boost converter is greatest. At this point (Vin=0) the inductor current is given by the ratio of the converter output voltage and the inductance (Vo/L). This current flows through the current sense resistor Rs and produces a voltage

with the slope VoRs/L (with current sense transformers it will be VoRs/NL). This slope, multiplied by the gain of the current error amplifier at the switching frequency, must be equal to the slope of the oscillator ramp (also in volts per second) for proper compensation of the current loop. If the gain is too high the slope of the inductor current will be greater than the ramp and the loop can go unstable. The instability will occur near the cusp of the input waveform and will disappear as the input voltage increases.

The loop crossover frequency can be found from the above equation if the gain of the current error amplifier is multiplied with it and it is set equal to one. Then rearrange the equation and solve for the crossover frequency. The equation becomes:

$$fci = \frac{Vout \times Rs \times Rcz}{Vs \times 2\pi L \times Rci}$$

Where fci is the current loop crossover frequency and Rcz/Rci is the gain of the current error amplifier. This procedure will give the best possible response for the current loop.

In the example converter the output voltage is 400Vdc and the inductor is 1.0mH so the down slope of inductor current is 400mA per microsecond. The current sense resistor is 0.25 ohms so the input to the current error amplifier is 100mV per microsecond. The oscillator ramp of the UC3854 has a peak to peak value of 5.2V and the switching frequency is 100KHz so the ramp has a slope of 0.52 volts per microsecond. The current error amplifier must have a gain of 5.2 at the switching frequency to make the slopes equal. With an input resistor (Rci) value of 3.9K the feedback resistance (Rcz) is 20K to give the amplifier a gain of 5.2. The current loop crossover frequency is 15.9KHz.

The placement of the zero in the current error amplifier response must be at or below the crossover frequency. If it is at the crossover frequency the phase margin will be 45 degrees. If the zero is lower in frequency the phase margin will be greater. A 45 degree phase margin is very stable, has low overshoot and has good tolerance for component variations. The zero must be placed at the crossover frequency so the impedance of the capacitor at that frequency must be equal to the value of Rcz. The equation is: Ccz = 1 / (2π x fci x Rcz). The example converter has Rcz=20K and fci=l5.9KHz so Ccz=500pF. A value of 620pF was chosen to give a little more phase margin.

A pole is normally added to the current error amplifier response near the switching frequency to reduce noise sensitivity. If the pole is above half the switching frequency the pole will not affect the frequency response of the control loop. The example converter uses a 62pF capacitor for Ccp which gives a pole at 128KHz. This is actually above the switching frequency so a larger value of capacitor could have been used but 62pF is adequate in this case.

Voltage Error Amplifier Compensation

The voltage control loop must be compensated for stability but because the bandwidth of the voltage loop is so small compared to the switching frequency the requirements for the voltage control loop are really driven by the need to keep the input distortion to a minimum rather than by stability. The loop bandwidth must be low enough to attenuate the second harmonic of the line frequency on the output capacitor to keep the modulation of the input current small. The voltage error amplifier must also have enough phase shift so that what modulation remains will be in phase with the input line to keep the power factor high.

The basic low frequency model of the output stage is a current source driving a capacitor. The power stage and the current feedback loop compose the current source and the capacitor is the output capacitor. This forms an integrator and it has a gain characteristic which rolls off at a constant 20dB per decade rate with increasing frequency. If the voltage feedback loop is closed around this it will be stable with constant gain in the voltage error amplifier. This is the technique which is used to stabilize the voltage loop. However, its performance at reducing distortion due to the second harmonic output ripple is miserable. A pole in the amplifier response is needed to reduce the amplitude of the ripple voltage and to shift the phase by 90 degrees. The distortion criteria is used to define the gain of the voltage error amplifier at the second harmonic of the line frequency and then the unity gain crossover frequency is found and is used to determine the pole location in the voltage error amplifier frequency response.

The first step in designing the voltage error amplifier compensation is to determine the amount of ripple voltage present on the output capacitor. The peak value of the second harmonic voltage is given by:

$$Vopk = \frac{Pin}{2\pi fr \times Co \times Vo}$$

Where Vopk is the peak value of the output ripple voltage (the peak to peak value will be twice this), fr is the ripple frequency which is the second harmonic of the input line frequency, Co is the value of the output capacitance and Vo is the DC output voltage. The example converter has a peak ripple voltage of 1.84Vpk.

The amount of distortion which the ripple contributes to the input must be decided next. This deci-

sion is based on the specification for the converter. The example converter is specified for 3% THD so 0.75% THD is allocated to this component. This means that the ripple voltage at the output of the voltage error amplifier is limited to 1.5%. The voltage error amplifier has an effective output range ($\Delta Vvea$) of 1.0 to 5.0 volts so the peak ripple voltage at the output of the voltage error amplifier is give by Vvea(pk) = %Ripple x $\Delta Vvea$. The example converter has a peak ripple voltage at the output of the voltage error amplifier of 60mVpk.

The gain of the voltage error amplifier, Gva, at the second harmonic ripple frequency is the ratio of the two values given above. The peak ripple voltage allowed on the output of the voltage error amplifier is divided by the peak ripple voltage on the output capacitor. For the example converter Gva is 0.0326.

The criteria for the choice of Rvi, the next step in the design process, are reasonably vague. The value must be low enough so that the opamp bias currents will not have a large effect on the output and it must be high enough so that the power dissipation is small. In the example converter a 511 K resistor was chosen for Rvi and it will have power dissipation of about 300mW.

Cvf, the feedback capacitor sets the gain at the second harmonic ripple frequency and is chosen to give the voltage error amplifier the correct gain at the second harmonic of the line frequency. The equation is simply:

$$Cvf = \frac{1}{2\pi fr \times Rvi \times Gva}$$

The example converter has a Cvf value of 0.08µF. If this value is rounded down to Cvf=0.047µF the phase margin will be a little better with only a little more distortion so this value was chosen.

The output voltage is set by the voltage divider Rvi and Rvd. The value of Rvi is already determined so Rvd is found from the desired output voltage and the reference voltage which is 7.50Vdc. In the example Rvd=l0K will give an output voltage of 390Vdc. This could be trimmed up to 400VDC with a 414K resistor in parallel with Rvd but for this application 390Vdc is acceptable. Rvd has no effect on the AC performance of the active power factor corrector. Its only effect is to set the DC output voltage.

The frequency of the pole in the voltage error amplifier can be found from setting the gain of the loop equation equal to one and solving for the frequency. The voltage loop gain is the product of the error amplifier gain and the boost stage gain, which can be expressed in terms of the input power. The multiplier, divider and squarer terms can all be lumped into the power stage gain and their effect is to transform the output of the voltage error amplifier into a power control signal as was noted earlier. This allows us to express the transfer function of the boost stage simply in terms of power. The equation is:

$$Gbst = \frac{Pin \times Xco}{\Delta Vvea \times Vo}$$

Where Gbst is the gain of the boost stage including the multiplier, divider and squarer, Pin is the average input power, Xco is the impedance of the output capacitor, $\Delta Vvea$ is the range of the voltage error amplifier output voltage (4 volts on the UC3854) and Vo is the DC output voltage.

The gain of the error amplifier above the pole in its frequency response is given by:

$$Gva = \frac{Xcf}{Rvi}$$

Where Gva is the gain of the voltage error amplifier, Xcf is the impedance of the feedback capacitance and Rvi is the input resistance.

The gain of the total voltage loop is the product of Gbst and Gva and is given by the this equation:

$$Gv = \frac{Pin \times Xco \times Xcf}{\Delta Vvea \times Vo \times Rvi}$$

Note that there are two terms which are dependent on f, Xco and Xcf. This function has a second order slope (-40dB per decade) so it must be a function of frequency squared. To solve for the unity gain frequency set Gv equal to one and rearrange the equation to solve for fvi. Xco is replaced with $1/(2\pi fCo)$ and Xcf is replaced with $1/(2\pi fCvf)$.

The equation becomes:

$$fvi^2 = \frac{Pin}{\Delta Vvea \times Vo \times Rvi \times Co \times Cvf \times (2\pi)^2}$$

Solving for fvi in the example converter gives fvi=19.14Hz. The value of Rvf can now be found by setting it equal to the impedance of Cvf at fvi. The equation is: $Rvf=1/(2\pi fviCvf)$.

In the example converter a value of 177K is calculated and 174K is used.

Feedforward Voltage Divider Filter Capacitors

The percentage of second harmonic ripple voltage on the feedforward input to the multiplier results in the same percentage of third harmonic ripple current on the AC line. The capacitors in the feedforward voltage divider (Cff1 and Cff2) attenuate the ripple voltage from the rectified input voltage. The

second harmonic ripple is 66.2% of the input AC line voltage. The amount of attenuation required, or the "gain" of the filter, is simply the amount of third harmonic distortion allocated to this distortion source divided by 66.2% which is the input to the divider. The example circuit has an allocation of 1.5% total harmonic distortion from this input so the required attenuation is Gff = 1.5 / 66.2 = 0.0227.

The recommended divider string impliments a second order filter because this gives a much faster response to changes in the RMS line voltage. Typically, it is about six times faster. The two poles of the filter are placed at the same frequency for the widest bandwidth. The total gain of the filter is the product of the gain of the two filter section so the gain of each section is the square root of the total gain. The two sections of the filter do not interact much because the impedances are different so they can be treated separately. In the example converter the gain of each filter section at the second harmonic frequency is 0.0227 or 0.15 for each section. This same relationship holds for the cutoff frequency which is needed to find the capacitor values. These are simple real poles so the cutoff frequency is the section gain times the ripple frequency or:

$$fc = \sqrt{Gff} \times fr$$

The example converter has a filter gain of 0.0227 and a section gain of 0.15 and a ripple frequency of 120Hz so the cutoff frequency is fc=0.15x120=18Hz.

The cutoff frequency is used to calculate the values for the filter capacitors since, in this applivation, the impedance of the capacitor will equal the impedance of the load resistance at the cutoff frequency. The two equations given below are used to calculate the two capacitor values.

$$Cff1 = \frac{1}{2\pi \times fp \times Rff2}$$

$$Cff2 = \frac{1}{2\pi \times fp \times Rff3}$$

In the example converter Rff2 is 91K and Rff3 is 20K; so,

Cff1=1/2πx18x91K=0.1μF;

Cff2=1/2πx18x20K=0.44μF;

so choose Cff2=0.47μF.

This completes the design of the major circuits of an active power factor corrector.

DESIGN PROCEDURE SUMMARY

This section contains a brief, step-by-step summary of the design procedure for an active power factor corrector. The example circuit used above is repeated here.

1. Specifications: Determine the operating requirements for the active power factor corrector.

   Example:

   Pout (max): 250W
   Vin range: 80-270Vac
   Line frequency range: 47-65Hz
   Output voltage: 400Vdc

2. Select switching frequency:

   Example:

   100KHz

3. Inductor selection:

   A. Maximum peak line current. Pin = Pout(max)

   $$Ipk = \frac{\sqrt{2} \times Pin}{Vin\ (min)}$$

   Example:

   Ipk=1.41 x250/80=4.42 amps

   B. Ripple current.

   $\Delta I = 0.2 \times Ipk$

   Example:

   ΔI=0.2x4.42= = 0.2x4.42 = 0.9 amps peak to peak

   C. Determine the duty factor at Ipk where Vin(peak) is the peak of the rectified line voltage at low line.

   $$D = \frac{Vo - Vin\ (peak)}{Vo}$$

   Example:

   D=(400-113)/400=0.71

   D. Calculate the inductance. fs is the switching frequency.

   $$L = \frac{Vin \times D}{fs \times \Delta I}$$

   Example:

   L=(113x.71)/(100,000x0.9)=0.89mH

   Round up to 1.0mH.

4. Select output capacitor. With hold-up time, use the equation below. Typical values for Co are 1 μF to 2μF per watt. If hold-up is not required use the second harmonic ripple voltage and total capacitor power dissipation to determine minimum size of the capacitor. Δt is the hold-up time in seconds and V1 is the minimum output

capacitor voltage.

$$Co = \frac{2 \times Pout \times \Delta t}{Vo^2 - V1^2}$$

Example:

Co=(2x250x34msec)/(400-350)=450µF

5. Select current sensing resistor. If current transformers are used then include the turns ratio and decide whether the output will be positive or negative relative to circuit common. Keep the peak voltage across the resistor low. 1.0V is a typical value for Vrs.

A. Find $Ipk(max) = Ipk + \frac{\Delta I}{2}$

Example:

Ipk(max)=4.42+0.45 ≈ 5.0amps peak

B. Calculate sense resistor value.

$$Rs = \frac{Vrs}{Ipk(max)}$$

Example:

Rs=1.0/5.0=0.20 ohms. Choose 0.25ohms

C. Calculate the actual peak sense voltage.

Vrs(pk)=Ipk(max)xRs

Example:

Vrs(pk)=5.0x0.25=1.25V

6. Set independent peak current limit. Rpk1 and Rpk2 are the resistors in the voltage divider. Choose a peak current overload value, Ipk(ovld). A typical value for Rpk1 is 10K.

$$Vrs(ovld) = Ipk(olvd) \times Rs$$

Example:

Vrs(ovld)=5.6x0.25=1.4V

$$Rpk2 = \frac{Vrs(ovld) \times Rpk1}{Vref}$$

Example:

Rpk2=(1.4x10K)/7.5=1.87K. Choose 1.8K

7. Multiplier setup. The operation of the multiplier is given by the following equation. Imo is the multiplier output current, Km=1 , Iac is the multiplier input current, Vff is the feedforward voltage and Vvea is the output of the voltage error amplifier.

$$Imo = \frac{Kmx Iacx(Vvea-1)}{vff^2}$$

A. Feedforward voltage divider. Change Vin from RMS voltage to average voltage of the rectified input voltage. At Vin(min) the voltage at Vff should be 1.414 volts and the voltage at Vffc, the other divider node, should be about 7.5 volts. The average value of Vin is given by the following equation where Vin(min) is the RMS value of the AC input voltage:

$$Vin(av) = Vin(min) \times 0.9$$

The following two equations are used to find the values for the Vff divider string. A value of 1 Megohm is usually chosen for the divider input impedance. The two equations must be solved together to get the resistor values.

$$vff = 1.414v = \frac{Vin(av) \times Rff3}{Rff1 + Rff2 + Rff3}$$

$$Vnode \approx 7.5V = \frac{Vin(av) x (Rff2+Rff3)}{Rff1 + Rff2 + Rff3}$$

Example:

Rff1=910K, Rff2=91K, and Rff3=20K

B. Rvac selection. Find the maximum peak line voltage.

$$Vpk(max) = \sqrt{2} \times Vin(max)$$

Example:

Vpk(max)=1.414x270=382Vpk

Divide by 600 microamps, the maximum multiplier input current.

$$Rvac = \frac{Vpk(max)}{600E-6}$$

Example:

Rvac=(382)/6E-4=637K. Choose 620K

C. Rb1 selection. This is the bias resistor. Treat this as a voltage divider with Vref and Rvac and then solve for Rb1. The equation becomes:

Rb1 = 0.25 Rvac

Example:

Rb1=0.25Rvac=155K. Choose 150K

D. Rset selection. Imo cannot be greater than twice the current through Rset. Find the multiplier input current, Iac, with Vin(min). Then calculate the value for Rset based on the value of Iac just calculated.

$$Iac(min) = \frac{Vin(pk)}{Rvac}$$

Example:

Iac(

$$Rset = \frac{3.75}{2 \times Iac(min)}$$

Example:

Rset=3.75V/(2x182μA)=10.3Kohms.

Choose 10 Kohms

E. Rmo selection. The voltage across Rmo must be equal to the voltage across Rs at the peak current limit at low line input voltage.

$$Rmo = \frac{Vrs\ (pk)\ x\ 1.12}{2\ x\ Iac(min)}$$

Example:

Rmo=(l.25x1.12)/(2x182E-6)=3.84K.

Choose 3.9Kohms

8. Oscillator frequency. Calculate Ct to give the desired switching frequency.

$$Ct = \frac{1.25}{Rset\ x\ fs}$$

Example:

Ct=1.25/(10K x 100K)=1.25nF.

9. Current error amplifier compensation.

A. Amplifier gain at the switching frequency. Calculate the voltage across the sense resistor due to the inductor current downslope and then divide by the switching frequency. With current transformers substitute (Rs/N) for Rs. The equation is:

$$\Delta Vrs = \frac{Vo \times Rs}{L \times fs}$$

Example:

ΔVrs=(400x0.25)/(0.001 =(400x0.25)/(0.001 x100,000)=1.0Vpk

This voltage must equal the peak to peak amplitude of Vs, the voltage on the timing capacitor (5.2 volts). The gain of the error amplifier is therefore given by:

$$Gca = \frac{Vs}{\Delta Vrs}$$

Example:

Gca=5.2/1.0=5.2

B. Feedback resistors. Set Rci equal to Rmo.

Rci = Rmo

Rcz = Gca x Rci

Example:

Rcz=5.2x3.9K=20Kohms

C. Current loop crossover frequency.

$$fci = \frac{Vout \times Rs \times Rcz}{Vs \times 2\pi L \times Rci}$$

Example:

fci=(400x0.25x20K)/(5.2x2πx0.001

=15.7KHz

D. Ccz selection. Choose a 45 degree phase margin. Set the zero at the loop crossover frequency.

$$Ccz = \frac{1}{2\pi \times fci \times Rcz}$$

Example:

Ccz=1/(2πx15.7Kx20K)=507pF.

Choose 620pF

E. Ccp selection. The pole must be above fs/2.

$$Ccp = \frac{1}{2\pi \times fs \times Rcz}$$

Example:

Ccp=1/(2πx1 100Kx20K)=80pf.

Choose 62pF

10. Harmonic distortion budget. Decide on a maximum THD level. Allocate THD sources as necessary. The predominant AC line harmonic is third. Output voltage ripple contributes 1/2% third harmonic to the input current for each 1% ripple at the second harmonic on the output of the error amplifier. The feedforward voltage, Vff, contributes 1% third harmonic to the input current for each 1% second harmonic at the Vff input to the UC3854.

Example:

3% third harmonic AC input current is chosen as the specification. 1.5% is allocated to the Vff input and 0.75% is allocated to the output ripple voltage or 1.5% to Vvao. The remaining 0.75% is allocated to miscellaneous nonlinearities.

11. Voltage error amplifier compensation.

A. Output ripple voltage. The output ripple is given by the following equation where fr is the second harmonic ripple frequency:

$$Vo\ (pk) = \frac{Pin}{2\pi fr \times Co \times Vo}$$

Example:

Vo(pk)=250/(2π120x450E-6x400)=1.84Vac

B. Amplifier output ripple voltage and gain. Vo(pk) must be reduced to the ripple voltage allowed at the output of the voltage error amplifier. This sets the gain of the voltage error amplifier at the second harmonic frequency. The equation is:

$$Gva = \frac{\Delta Vvao \times \%Ripple}{Vo\ (pk)}$$

For the UC3854 Vvao is 5-1=4V

Example:

Gva=(4x0.015)/1.84=0.0326

C. Feedback network values. Find the component values to set the gain of the voltage error amplifier. The value of Rvi is reasonably arbitrary.

Example:

Choose Rvi=511K

$$Cvf = \frac{1}{2\pi \times fr \times Rvi \times Gva}$$

Example:

Cvf=1/(2πx120x511Kx0.0326)=0.08μF.

Choose 0.047μF

D. Set DC output voltage.

$$Rvd = \frac{Rvi \times Vref}{Vo - Vref}$$

Example:

Rvd=(511Kx7.5)/(400-7.5)=9.76K.

Choose 10.0K

E. Find pole frequency. fvi = unity gain frequency of voltage loop.

$$fvi^2 = \frac{Pin}{\Delta Vvao \times Vo \times Rvi \times Co \times Cvf \times (2\pi)^2}$$

Example:

$$fvi = \sqrt{(250/(4x400x511Kx450E-6x47E-9x39.5))} =$$

19.1 Hz

F. Find Rvf.

$$Rvf = \frac{1}{2\pi \times fvi \times Cvf}$$

Example:

Rvf=1/(2πx19.1 x47E-9)=177K. Choose 174K

12. Feedforward voltage divider capacitors. These capacitors determine the contribution of Vff to the third harmonic distortion on the AC input current. Determine the amount of attenuation needed. The second harmonic content of the rectified line voltage is 66.2%. %THD is the allowed percentage of harmonic distortion budgeted to this input from step 10 above.

$$Gff = \frac{\%THD}{66.2\%}$$

Example:

Gff=1.5/66.2=0.0227

Use two equal cascaded poles. Find the pole frequencies. fr is the second harmonic ripple frequency.

$$fp = \sqrt{Gff} \times fr$$

Example:

fp=0.15xl20=18Hz

Select Cff1 and Cff2.

$$Cff1 = \frac{1}{2\pi \times fp \times Rff2}$$

$$Cff2 = \frac{1}{2\pi \times fp \times Rff3}$$

Example:

Cff1=1/(2πx18x91K)=0.097μF. Choose 0.10μF

Cff2=1/(2πx18x20K)=0.44μF. Choose 0.47μF

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